(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 720 023 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
03.07.1996 Bulletin 1996/27

(51) Int. Cl.[6]: **G01R 31/00**, G01R 31/316

(21) Application number: **94830592.5**

(22) Date of filing: **30.12.1994**

(84) Designated Contracting States:
DE FR GB IT

(71) Applicant: **SGS-THOMSON MICROELECTRONICS S.r.l.**
I-20041 Agrate Brianza (Milano) (IT)

(72) Inventors:
- **Brambilla, Davide**
  I-20017 Rho (Milano) (IT)
- **Capodivacca, Giovanni**
  I-21053 Castellanza (VA) (IT)
- **Stefani, Fabrizio**
  I-21010 Cardano al Campo (VA) (IT)

(74) Representative: **Checcacci, Giorgio**
PORTA, CHECCACCI & BOTTI s.r.l.
Viale Sabotino, 19/2
I-20135 Milano (IT)

(54) Test method for power integrated devices

(57) A method of checking the integrity of an electric power connect (7) between a contact pad (5) of an integrated circuit (2) and a corresponding contact pin (8) in an electronic power device including two final power stages (3,4) powered from respective discrete contact pads (5,6) connected by means of electric power connects (7,13) to respective contact pins (8,9), comprises the steps of,

- providing a resistive connection (14) between said two contact pads (5,6),
- bringing a first final power stage (3), powered from the first contact pad (5), to a conduction state,
- measuring the potential difference between the two contact pins (8,9) connected to said two contact pads (5,6), and
- comparing said potential difference with a predetermined nominal potential difference.

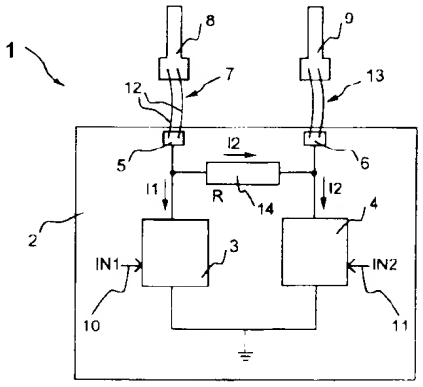

FIG.2

EP 0 720 023 A1

Description

Field of the Invention

This invention relates to a method of testing integrated power devices, and in particular, to a method of checking the integrity of a two-wire electric connect between a contact pad of an integrated power circuit encapsulated within a package and a corresponding contact pin made available on the package exterior.

The invention concerns in particular an integrated power circuit of the type which either comprises a power stage and signal stage or two final power stages which are structurally independent and powered through respective discrete contact pads connected by two-wire electric connects to respective pins of the package, and a means of testing such two-wire connects for integrity.

Background Art

As is known, in integrated power circuits, the connections between certain contact pads of the integrated circuit and corresponding metallic contact pins of the package are provided by two wires in parallel, in order to increase the maximum current that the connection can accommodate. In this way, the two wires in parallel can accommodate currents of upward of 5 Amps.

For electronic devices which have more than one final power stage, such as certain audio amplifiers which may draw still larger currents, it is preferred that the power connection be split by having each final stage connected to its corresponding supply contact pin by a two-wire connect. In normal operation of the device, there would be at least two supply contact pins connected to the same electric potential, that is, either to the supply voltage or the circuit ground.

It matters to observe that, at the end of the fabricating process that yields the integrated power device product, the metallic pins will only be accessible on the package exterior.

Thus, there exists a need to ascertain the integrity and soundness of the two-wire connect welds, in view of current welding processes yielding a rate of rejects of 50 to 100 ppm (pieces per million). Conventional measuring methods have been in use which provide automatic checking capabilities, and specifically, a measurement of pin-to-pin continuity. Such methods, however, have been unable to discriminate between a faulty connect, wherein a single wire is present, and a sound connect, wherein both wires are present, because the resistance of gold wires is negligible compared to the overall resistance of the circuit being measured.

To overcome this problem, the prior art has proposed a first solution which consists of splitting the contact pad of the integrated circuit into two separate subpads connected to the same pin by respective wire connects. This solution allows of conventional testing, but has a disadvantage in that it requires that the area of the integrated circuit be expanded to accommodate the increased number of contact pads provided. This is undesirable in that the present trend favors enhanced miniaturization of integrated circuits and devices. In addition, certain technological restrictions from the layout rules make this solution impracticable.

Disclosed in European Patent Application 93830186.8, published on November 2, 1994 under No. 0622733, is a second solution, in particular a method of testing two-wire electric connects in integrated power devices. This method provides for a first contact pad, to which a two-wire connect to be checked for integrity is run, to be connected, via a power diode formed within the integrated circuit, to a second pad made available on the device exterior.

By having a large (a few Amps) current flowed beetween the two device contact pins connected to said contact pads, and therefore through the power diode, a power dissipation by the wire connects between the pins and the pads is caused. As is known, a rise in the wire temperature results in the resistance of the wires also increasing in value. Thus, by sampling the change in voltage across the two pins over time, which voltage would vary with the resistance of the wire connects, and comparing such samplings with values obtained by testing a sample device, it becomes possible to tell an intact two-wire connect from a faulty single-wire one.

In general, the last-mentioned method is used for checking the two-wire connects provided at the outputs of power amplifiers since, between the output pad of the final stage and the circuit ground, an intrinsic p-n junction is present which is normally reverse biased. This junction is part of the integrated structure of the final power transistor. Accordingly, it has been found advantageous to use this junction for continuity checks on the two-wire connect at that output. On the other hand, in order to check a two-wire connect provided at a supply contact pin of a power device by this method, it would be necessary to integrate a diode to the integrated circuit which can accommodate currents on the order of 5 Amps, that is a diode of a fairly large size. Where devices having several final power stages powered from different supply pins are involved, it would be necessary to integrate a power diode for each supply pin. Thus, the area of the integrated circuit would be greatly increased by the introduction of components which only are of use for testing purposes.

The underlying technical problem of this invention is to provide a method of checking the integrity of a two-wire electric power connect between a contact pad of an integrated circuit encapsulated within a package and a corresponding contact pin, which method allows said connect to be checked from outside the device, in a very short time and without involving any integration of power components to the integrated circuit which would only come useful at a testing stage.

This technical problem is solved by a testing method as defined in Claims 1 to 4 and 7 to 9.

The problem is also solved by an integrated device as defined in Claims 5, 6, 10 and 11.

The features of this invention will become apparent from the following detailed description of an embodiment thereof shown, by way of non-limitative example, in the accompannying drawings of which,

Figure 1 is a diagram showing schematically a power device of a known type which has two final stages with independent power supplies;

Figure 2 is a diagram showing schematically a first power device according to the invention, to which the following method is applied; and

Figure 3 is a diagram showing schematically a second power device according to the invention, to which the following method is applied.

Detailed Description

Shown in Figure 1 is a portion of an electronic power device 1 which incorporates an integrated circuit 2 comprising two final stages 3 and 4 which are independently powered through two contact pins 8 and 9 on the device 1.

In particular, two electric power connects 7 and 13 are shown formed between respective contact pads 5 and 6 of the integrated circuit 2 and corresponding contact pins 8 and 9.

These electric power connects 7 and 13 are two-wire connects, each formed by welding two gold wires 12 on the contact pads 5, 6 of the integrated circuit 2, with one end, and on the contact pins 8, 9 of the device 1, with the other end.

In the device depicted in the Figure, both two-wire connects 7 and 13 are used for connecting the final stages 3 and 4 to a positive pole of the supply generator, but could be used in a similar way for connection to a further voltage reference, such as the electric ground of the circuit.

The two final stages 3 and 4 can be driven via two inputs 10 and 11. Thus, each final stage can be brought to a conducting state or a cut-off state in an independent manner, from outside the device.

Shown in Figure 2 is a portion of a power device 1 incorporating an integrated circuit 2 which has two final stages 3 and 4 with independent power supplies, and including a means 14 of testing two-wire electric connects for integrity in accordance with the invention.

The two-wire connects 7 and 13, used for powering the two final stages 3 and 4, are to be checked for integrity. Advantageously, the two contact pads 5 and 6 of the integrated circuit 2 are interconnected by an integrated resistive element 14. This resistive element 14 should have a very low value resistance, e.g. 10 Ohms, and as explained hereinafter, has very small currents (tens of milliamps) flowed therethrough. Accordingly, it can be formed on the integrated circuit in a region of greatly reduced area, where a certain type, e.g. N type, of dopant is diffused.

In particular, the following method is once used to check the first two-wire connect 7 for integrity, and a second time to check the second two-wire connect 13 for integrity.

The first step of the method provides for the device 1 to be powered through the supply contact pin 8, which pin powers the first final stage 3 directly.

The second final stage 4, moreover, is powered through the integrated resistive element 14.

While holding the second final stage 4 in the cut-off state, the first final stage 3 is brought to a state of enhanced conduction by having it draw a large, 4 to 5 Amps, current I1 through the supply pin 8.

Thus, the second final stage will draw, via the resistor 14, a very small current I2, in the 50 mA range.

The current drawn by the supply generator and flowed through the two-wire connect 7 is the sum of the two currents I1 and I2 drawn by the two final stages, and closely approaches the current I1 in magnitude.

The second step of the inventive method consists of measuring the potential difference between the two supply pins 8 and 9 of the two final stages. This potential difference is the sum of the voltage drop across the two gold wires of the power connect 7 and the voltage drop across the resistive element 14, given that no current will be flowing through the second power connect 13, so that the potential drop is null thereacross.

The potential difference between the two pins 8 and 9 is given by the following formula, referred to as formula A hereinafter:

$$V = (I1 + I2)*Rwire + I2*R \qquad (A)$$

where, Rwire is the resistance of the power connect 7, and R is the resistance of the integrated resistive element 14.

Listed in the chart below are some exemplary values for the electrical quantities used in formula A, respectively in the case of a two-wire connect and a faulty single-wire connect:

	2-wire	1-wire	
I1	5	5	Amps
I2	.05	.05	Amps
Rwire	11E-3	22E-3	Ohms
R	10	10	Ohms

From these values, the value of the voltage V can be calculated for either cases:

V1 = (5+0.05)*11E-3+0.05*10 = 0.555 Volts

V2 = (5+0.05)*22E-3+0.05*10 = 0.611 Volts

It can be seen that the two voltages V1 and V2 differ by 55 millivolts from each other; therefore, by comparing the voltage value V measured on the piece being tested with a value previously measured on a sample piece, a good two-wire connect can be discriminated from a faulty single-wire connect.

Using the same procedure, the second two-wire connnect 13 can be checked for integrity by powering the device 1 through the supply pin 9 which powers the second final stage 4 directly.

Consequently, the first final stage 3 will be powered via the integrated resistive element 14.

Thereafter, while holding the first final stage 3 in the cut-off state, the second final stage 4 is brought to a state of enhanced conduction, and the potential difference between the two supply pins 8 and 9 of the two final stages measured.

By comparing this voltage value with a value previously measured on a sample piece, a good two-wire connect can be discriminated from a faulty single-wire connect, similar to the foregoing instance.

To summarize, the above-described method and device allow devices wherein a wire is missing from or damaged in the two-wire connect, to be located in a positive manner. Thus, a high degree of quality and reliability can be ensured for the pieces that tested good. These results are obtained at a significant saving in area of the integrated circuit compared to prior art solutions.

In particular, the solution described requires very simple testing equipment, and the test can be completed in a very short time.

It will also be appreciated that changes and modifications may be made unto the method and device herein described and illustrated, without departing from the protection scope of this invention. In particular, it should be emphasized that the method used can be applied to any pair of equipotential contact pins on the device; more specifically, it can be used to check power connects between two ground contact pads of the integrated circuit and two respective ground contact pins on the device.

As an example, this method may be applied to a power device 1, shown schematically in Figure 3, which incorporates an integrated circuit 2 having a final power stage 3 and a signal stage 15 powered through two independent equipotential contact pins 8 and 18, and including a means 14 of checking a two-wire electric connect for integrity.

The connect 7 between the contact pad 5, through which the power stage 3 is powered, and the contact pin 8 is provided by a double wire 12, whereas the connect 19 between the contact pad 17, through which the signal stage 15 is powered, and the contact pin 18 is provided by a single wire.

Advantageously, the two contact pads 5 and 18 of the integrated circuit 2 are connected to each other through an integrated resistive element 14.

In order to check the two-wire electric connect 7 for integrity, the device 1 is powered through the supply pin 8, which pin powers the final stage 3 directly.

The signal stage 15 will, therefore, be powered through the integrated resistive element 14, and will draw a small current, denoted by I2 in the Figure, via this resistor 14.

The final power stage 3 is then brought to a state of enhanced conduction, causing it to draw a large current I1 from the supply pin 8, and the potential difference between the two pins 8 and 9 is measured.

By comparing this voltage value with a value previously measured on a sample piece, a good two-wire connect can be discriminated from a faulty single-wire connect, the same as in the previously described embodiment.

Claims

1. A method of checking the integrity of an electric power connect (7) between at least one contact pad (5) of an integrated circuit (2) encapsulated within a package and a corresponding contact pin (8), said integrated circuit (2) including at least two final power stages (3,4) powered from respective discrete contact pads (5,6) connected by means of electric power connects (7,13) to respective contact pins (8,9), characterized in that it comprises the steps of,

   - providing a resistive connection (14) between said two contact pads (5,6),
   - bringing a first final power stage (3), powered from the first contact pad (5), to a conduction state,
   - measuring the potential difference between the two contact pins (8,9) connected to said two contact pads (5,6), and
   - comparing said potential difference with a predetermined nominal potential difference.

2. A method according to Claim 1, characterized in that said resistive connection (14) is an integrated resistive element of low resistance value.

3. A method according to Claim 2, characterized in that, during the test, the second final power stage (4) of the integrated circuit (2) is held in a cut-off state and draws a known value current from the first contact pad through said integrated resistive element (14).

4. A method according to Claim 2, characterized in that said potential difference between said two contact pins (8,9) is the sum of the voltage drop across the electric power connect (7) between said first contact pad (5) and the corresponding contact pin (8) and the voltage drop across said integrated resistive element (14).

5. An integrated power device (1) including a means of checking the integrity of an electric power connect (7) between a contact pad (5) of an integrated circuit (2) incorporated thereto and a corresponding contact pin (8), said integrated circuit (2) including at least two final power stages (3,4) powered from two discrete contact pads (5,6) being independently connected to associated contact pins (8,9), characterized in that said contact pads (5,6) of the integrated circuit (2) are connected to each other through an integrated resistive element (14).

6. A device according to Claim 5, characterized in that said integrated resistive element (14) is a low resistance value element.

7. A method of checking the integrity of an electric power connect (7) between at least one contact pad (5) of an integrated circuit (2) encapsulated within a package and a corresponding contact pin (8), said integrated circuit (2) including at least one final power stage (3) and a signal stage (15) powered from respective discrete contact pads (5,17) connected through electrical connects (7,19) to respective contact pins (8,18), characterized in that it comprises the steps of,

   - providing a resistive connection (14) between said two contact pads (5,17),
   - bringing the final power stage (3) powered from the first contact pad (5) to a conduction state,
   - measuring the potential difference between the two contact pins (8,18) connected to said two contact pads (5,17), and
   - comparing said potential difference with a predetermined nominal potential difference.

8. A method according to Claim 7, characterized in that said resistive connection (14) is a low resistance value element.

9. A method according to Claim 8, characterized in that said potential difference between said two contact pins (8,18) is the sum of the voltage drop across the electric power connect (7) between said first contact pad (5) and the corresponding contact pin (8) and the voltage drop across said integrated resistive element (14).

10. An integrated power device including a means of checking the integrity of an electric power connect (7) between a contact pad (5) of an integrated circuit (2) incorporated thereto and a corresponding contact pin (8), said integrated circuit (2) including at least one final power stage (3) and a signal stage (15) powered from two discrete contact pads (5,17) independently connected to associated contact pins (8,18), characterized in that said contact pads (5,17) of the integrated circuit (2) are connected to each other through an integrated resistive element (14).

11. A device according to Claim 10, characterized in that said integrated resistive element (14) is a low resistance value element.

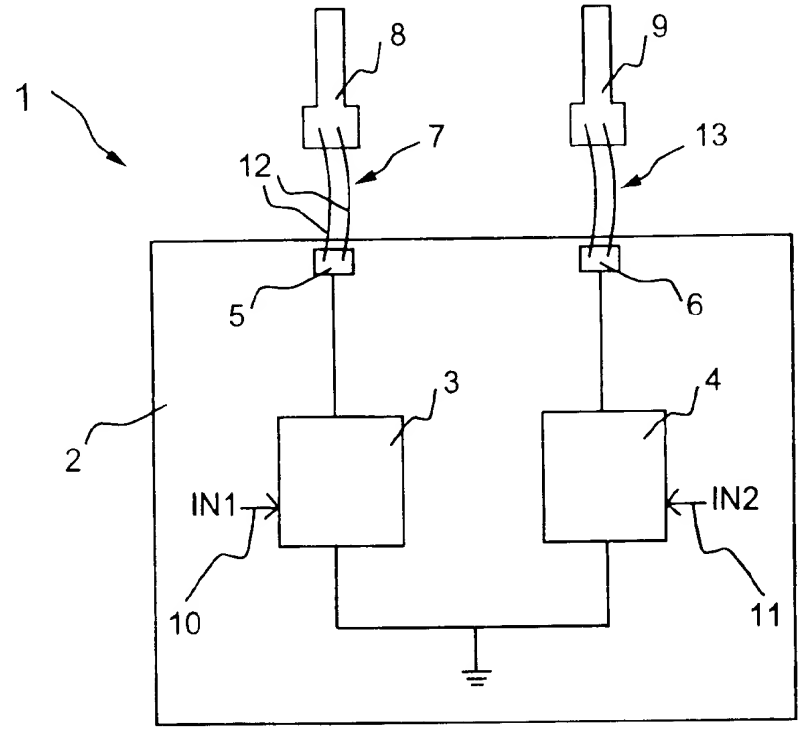
1
8
9
7
13
12
5
6
3
4
2
IN1
IN2
10
11

FIG.1

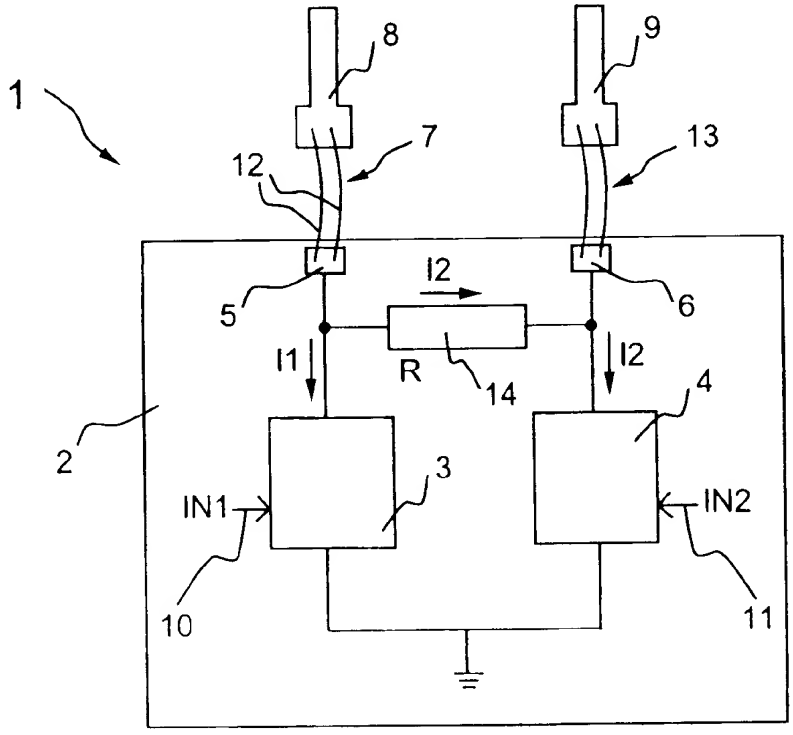
1
8
9
7
13
12
I2
5
6
I1
R
14
I2
4
2
3
IN1
IN2
10
11

FIG.2

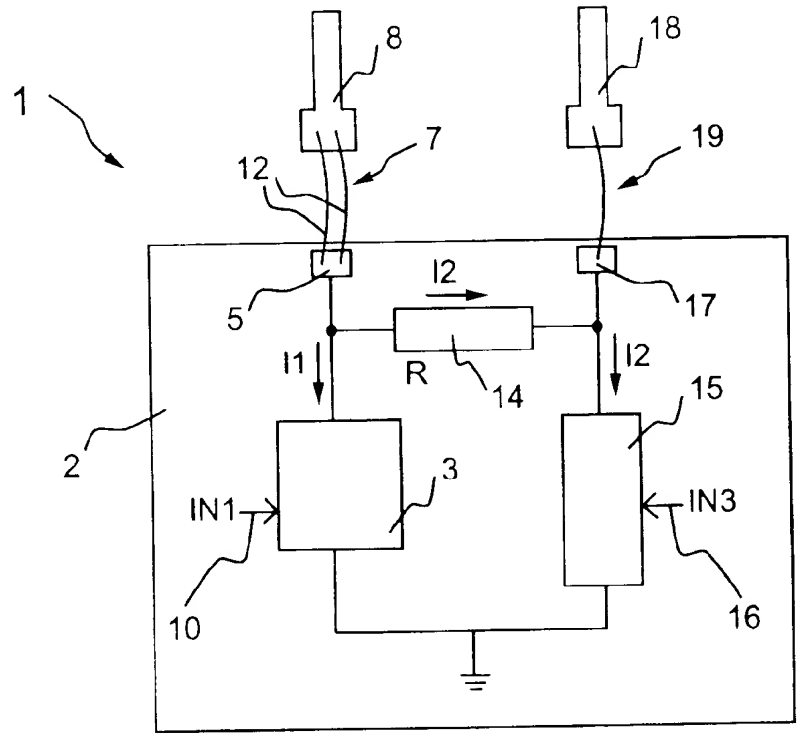

FIG.3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 83 0592

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
D,A	EP-A-0 622 733 (SGS-THOMSON)	1	G01R31/00 G01R31/316

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G01R

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 May 1995	Hoornaert, W

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)